In the Claims

Claims 1-15 are pending in the patent application, because the originally filed claims 16-20 were previously withdrawn.

1. (currently amended) A method comprising:

exposing a field of a semiconductor wafer having an alignment mark thereon using a full-image mask, such that the field, including the alignment mark thereon, is entirely exposed by an image of the mask; and,

performing a clear out process around the alignment mark on the field of the semiconductor wafer to reveal the alignment mark, including exposing just the alignment mark on the field using an auxiliary mask.

2. (original) The method of claim 1, wherein the full-image mask is a positive photoresist mask.

3. (original) The method of claim 1, wherein the field is located at an edge of the semiconductor wafer.

4. (original) The method of claim 1, wherein the field is located at one of an upper-right part and a lower-left part of an edge of the semiconductor wafer.

5. (original) The method of claim 1, further initially comprising depositing photoresist on the field of the semiconductor wafer.

6. (original) The method of claim 5, further comprising removing the photoresist that was exposed.

7. (original) The method of claim 6, wherein removing the photoresist that was exposed comprises developing the photoresist that was exposed.

8. (original) The method of claim 6, further comprising etching the semiconductor wafer.

9. (original) The method of claim 8, further comprising removing the photoresist that was unexposed.

10. (original) The method of claim 9, wherein removing the photoresist that was unexposed comprises stripping the photoresist that was unexposed.

11. (currently amended) A method for fabricating one or more semiconductor devices comprising:

exposing a field of a semiconductor wafer having an alignment mark thereon using a full-image mask, such that the field, including the alignment mark thereon, is entirely exposed by an image of the mask; and,

performing a clear out process around the alignment mark on the field of the semiconductor wafer to reveal the alignment mark, including exposing just the alignment mark on the field using an auxiliary mask,

such that the one or more semiconductor devices fabricated using the method have greater planar uniformity as compared to using a partial-image exposure process on the field to maintain the alignment mark.

12. (original) The method of claim 11, wherein the full-image mask is a positive photoresist mask.

13. (original) The method of claim 11, wherein the field is located at an edge of the semiconductor wafer.

14. (original) The method of claim 11, further comprising:

prior to exposing the field of the semiconductor wafer, depositing photoresist on the field of the semiconductor wafer; and,

developing the photoresist that was exposed.

15. (original) The method of claim 14, further comprising:

etching the semiconductor wafer; and,

stripping the photoresist that was unexposed.

16. (withdrawn) A semiconductor device formed at least in part by a method comprising:

depositing photoresist on a field of a semiconductor wafer having an alignment mark thereon;

exposing the photoresist on the field of the semiconductor wafer using a full-image mask inclusive of the alignment mark;

developing the photoresist on the field of the semiconductor wafer to remove exposed parts of the photoresist;

etching the semiconductor wafer;

stripping the photoresist that was unexposed; and

performing a clear out process around the alignment mark on the field of the semiconductor wafer to reveal the alignment mark.

17. (withdrawn) The device of claim 16, wherein the full-image mask is a positive photoresist mask.

18. (withdrawn) The device of claim 16, wherein the field is located at an edge of the semiconductor wafer.

19. (withdrawn) The device of claim 16, wherein the field is located at an upper-right part of an edge of the semiconductor wafer.

20. (withdrawn) The device of claim 16, wherein the field is located at a lower-left part of an edge of the semiconductor wafer.